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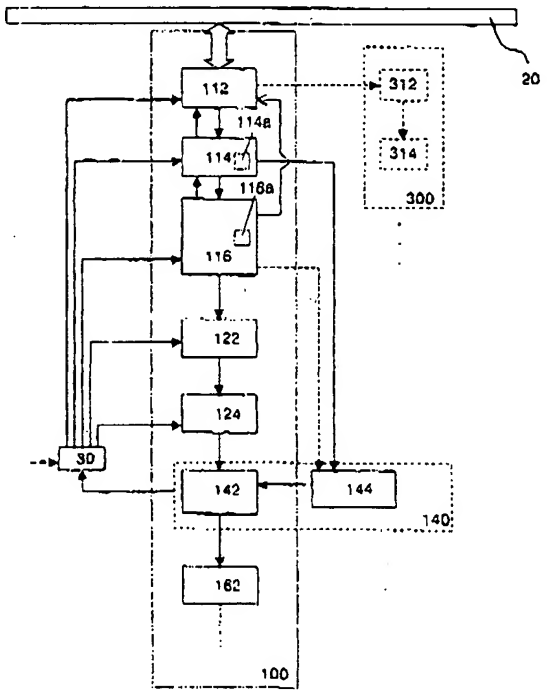
(54) Title: PIPELINED PROCESSOR AND INSTRUCTION LOOP EXECUTION METHOD



(57) Abstract: Processor (10) having a processing pipeline (100) is extended with an arrangement to reduce the loss of cycles associated with loop execution in pipeline (100). Loop start detection unit (116a) detects a loop start instruction containing information about the loop count and last instruction in the loop. Information about the first instruction in the loop is also present. Loop end detection unit (114a) is provided with the loop end information, and fetch stage (112) is provided with the loop start information by loop start detection unit (116a). Upon detection of a loop end, loop end detection unit (114a) triggers fetch stage (112) to fetch the first instruction of the loop. In addition, loop end detection unit (114a) generates detection tags labeling the content of pipeline (100), which are evaluated by tag detection unit (144). Loop execution control stage (142) compares the loop count information with detection information generated by tag detection unit (144) and, if necessary, removes superfluous instructions from pipeline (100).

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